Audio Registers

Currently for left channel ADC and DAC only.

Addresses defined in address\_map\_arm.h

**AUDIO\_CTRL 0xFF203040**

This is an 8-bit control register, write only.

Bit 0: dac\_sclr (synchronous clear the DAC fifo when =1)

Bit 1: dac\_wr (write a word to the DAC fifo when = 1; will only write once per rising edge of dac\_wr)

Bit 2: adc\_sclr (synchronous clear the ADC fifo when =1)

Bit 3: adc\_rd (read a word from the ADC fifo when = 1; will only read once per rising edge of dac\_wr)

**AUDIO\_SPACE 0xFF203050**

This is a 16-bit fifospace register, read only. Each FIFO has 128 16-bit words.

Bit 0: dac\_fifo\_empty

Bit 1: dac\_fifo\_half\_empty

Bit 2: dac\_fifo\_full

Bit 3: adc\_fifo\_empty

Bit 4: adc\_fifo\_half\_empty

Bit 5: adc\_fifo\_full

**AUDIO\_DAC\_LEFT\_DAT 0xFF203060**

This a 32-bit write register for writing the left channel data to the DAC. Once you set this to the desired output word, you will need to set the dac\_wr bit in the control register to a 1 and then to a 0 for the 32-bit word to be entered into the DAC FIFO.

**AUDIO\_ADC\_LEFT\_DAT 0xFF203070**

This a 32-bit read register for reading the left channel data from the ADC. To get a new word from the ADC FIFO, you will need to set the adc\_rd bit in the control register to a 1 and then to a 0.